

(Prior Art)

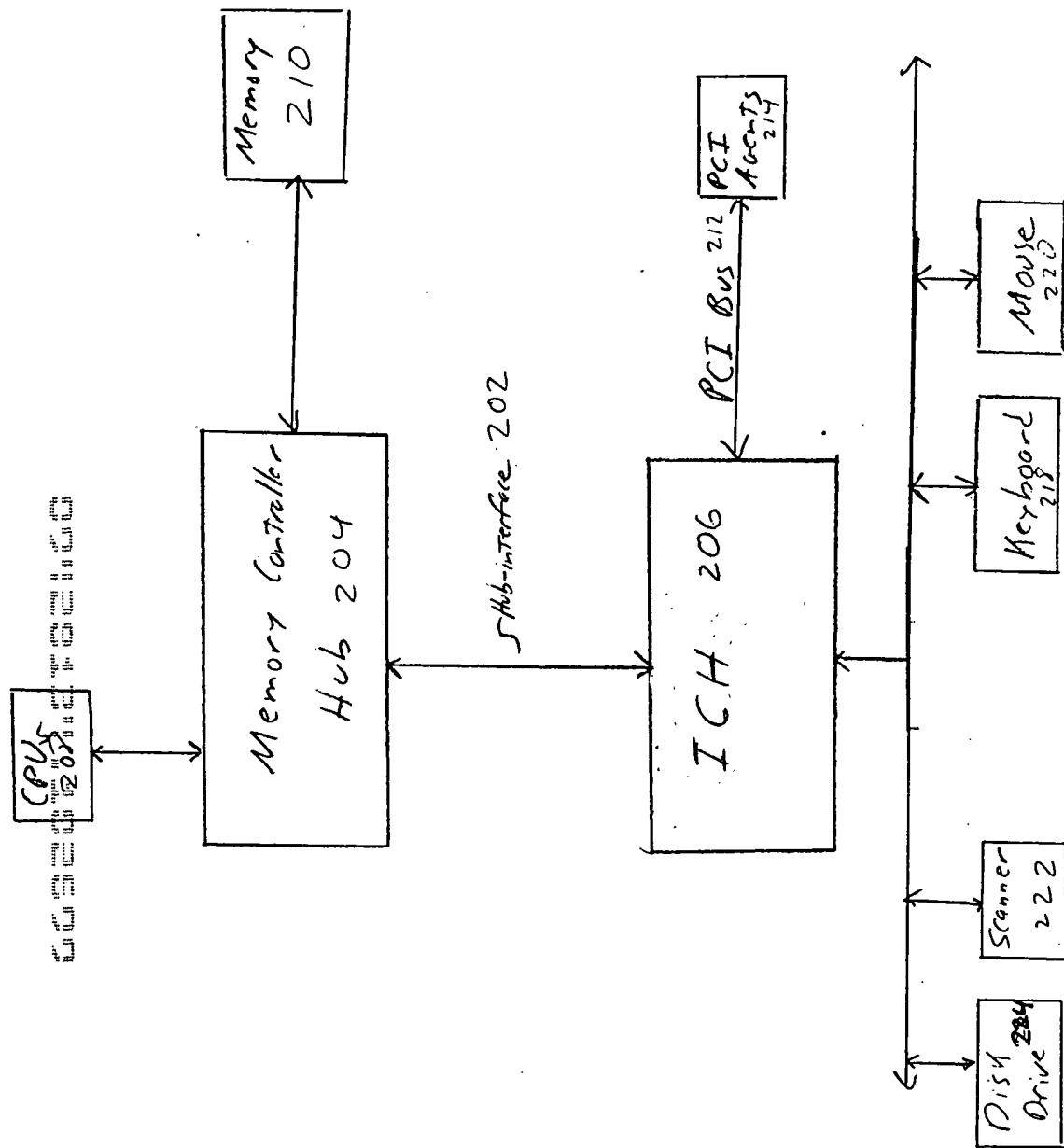


Fig. 2

FIG. 2 is a timing diagram illustrating the operation of the system in accordance with the present invention. The diagram shows the relationship between the HLCLK signal and the data transfer sequence.

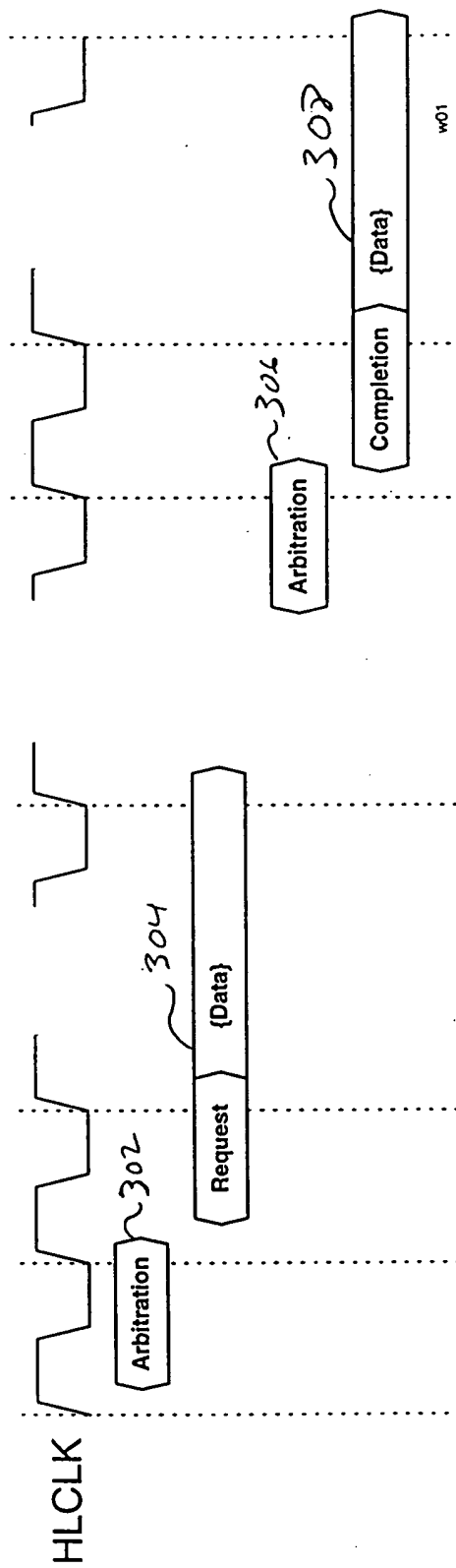


FIG. 2

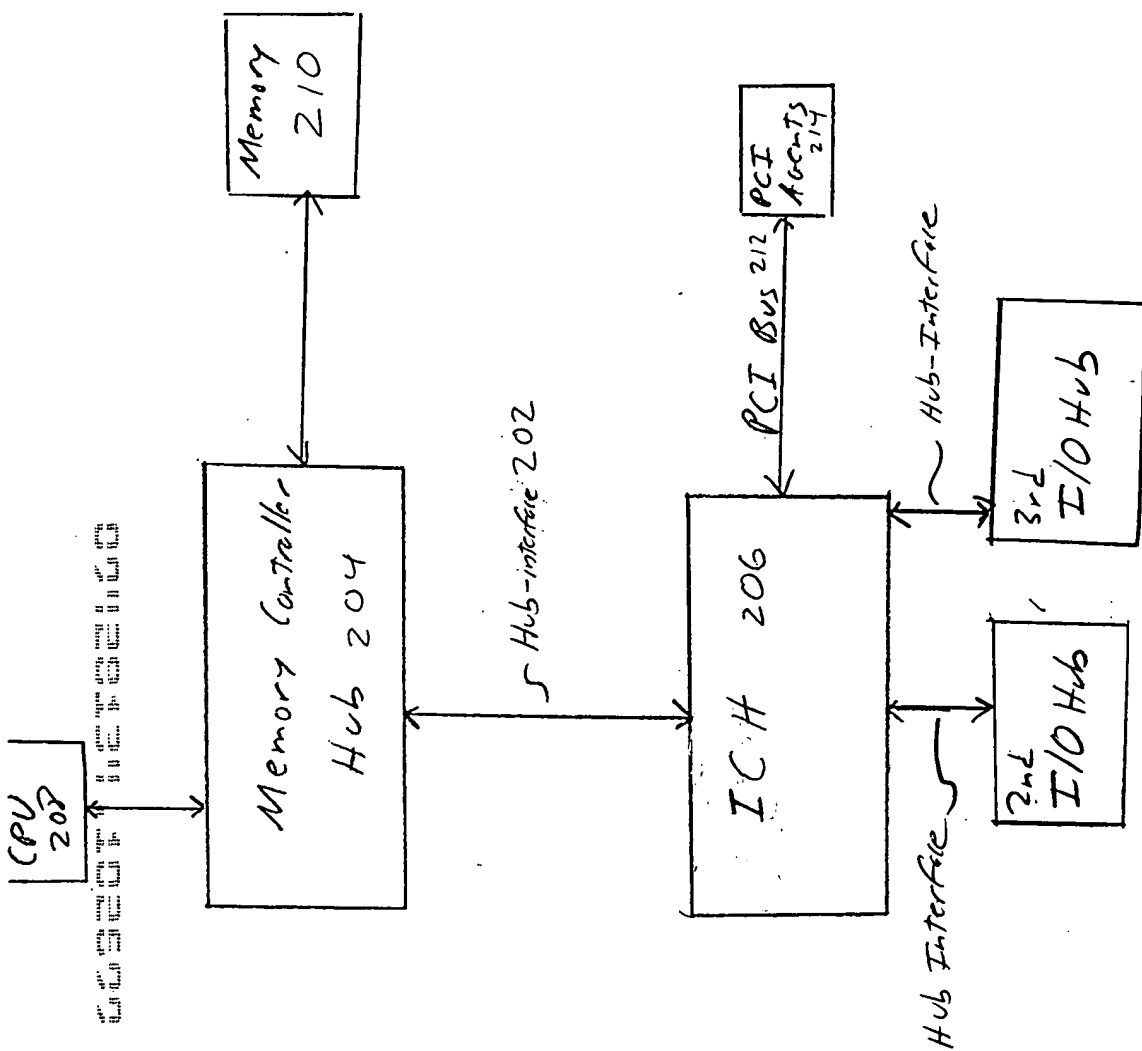


Fig. 4

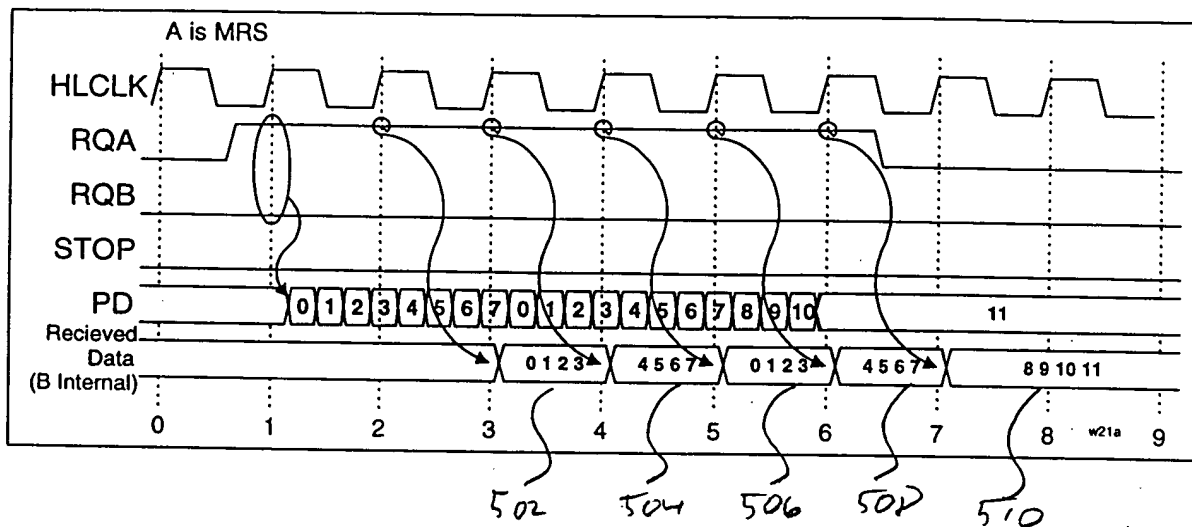


Fig. 5

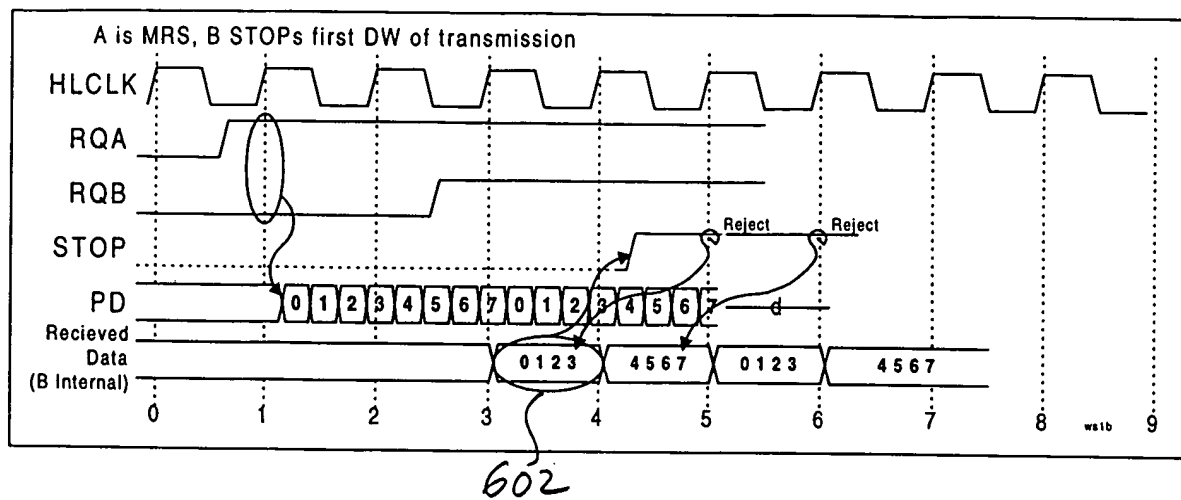


Fig. 6

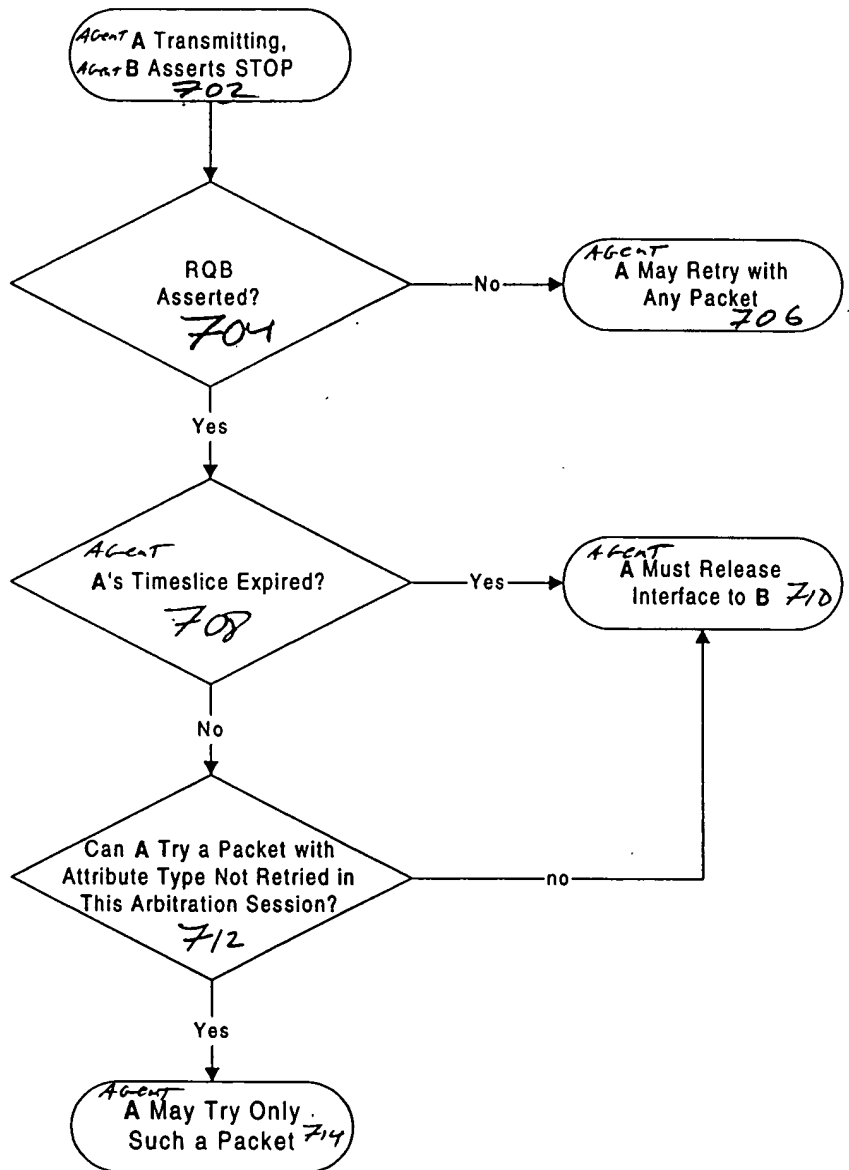


FIG. 7

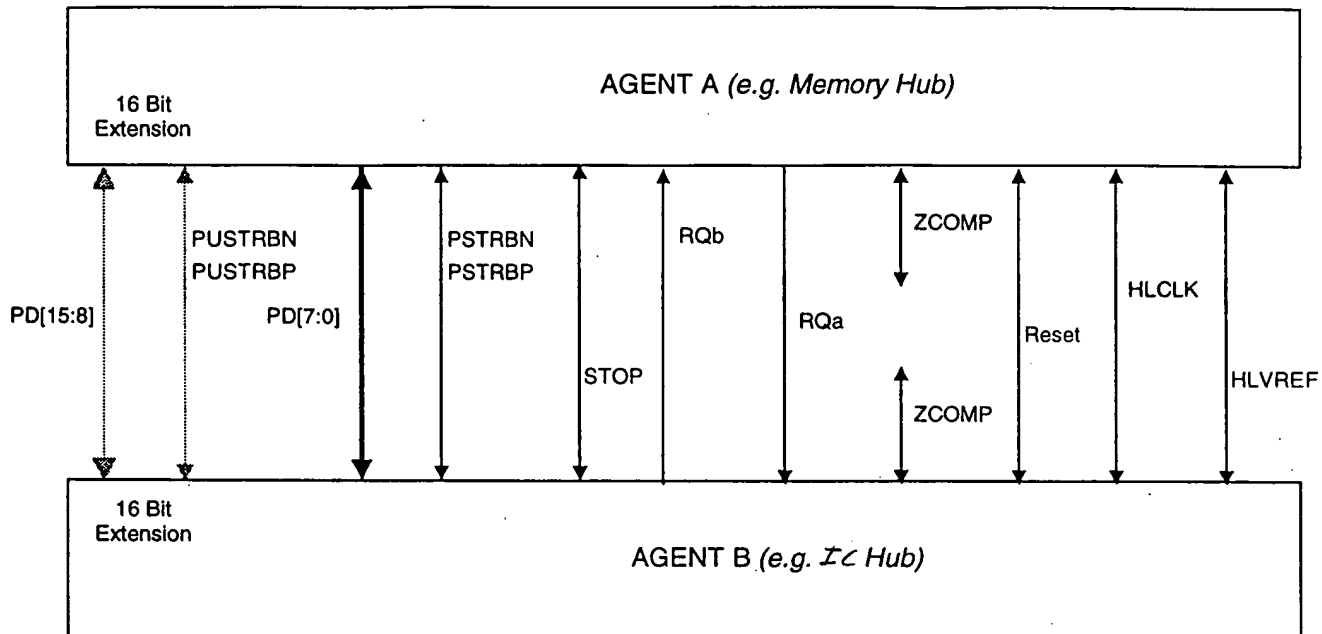


Fig. 8



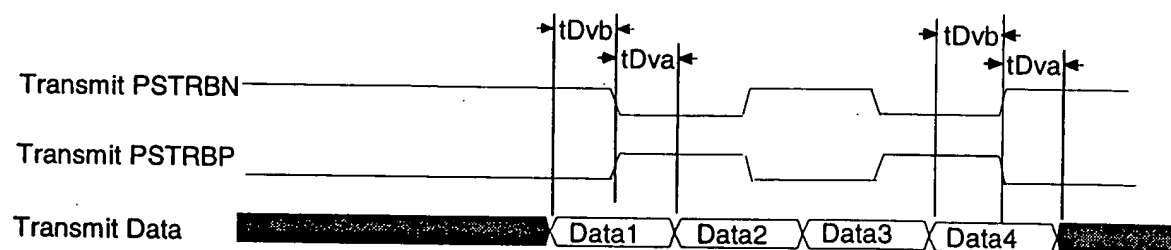


Fig. 9

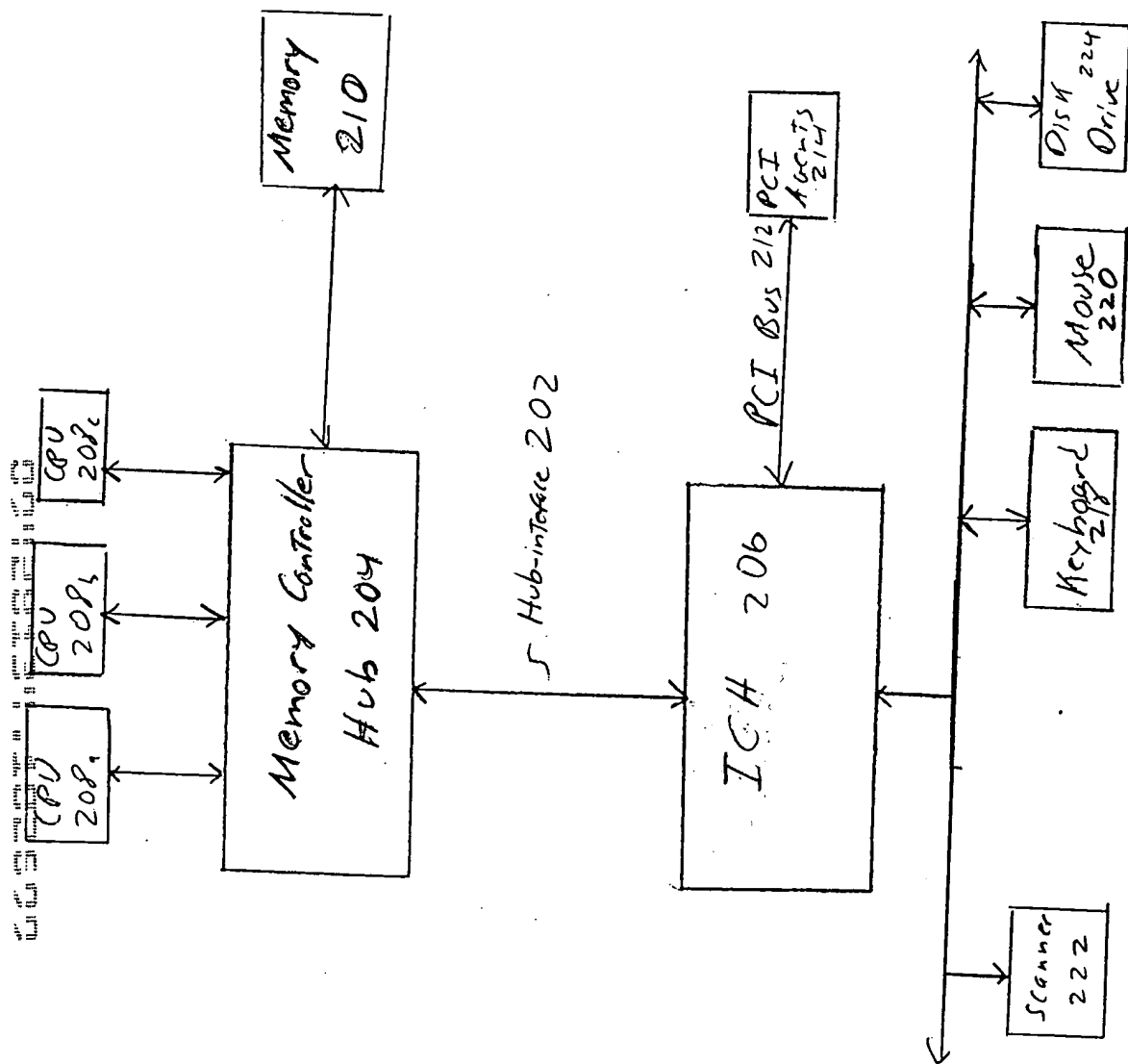


FIG. 10

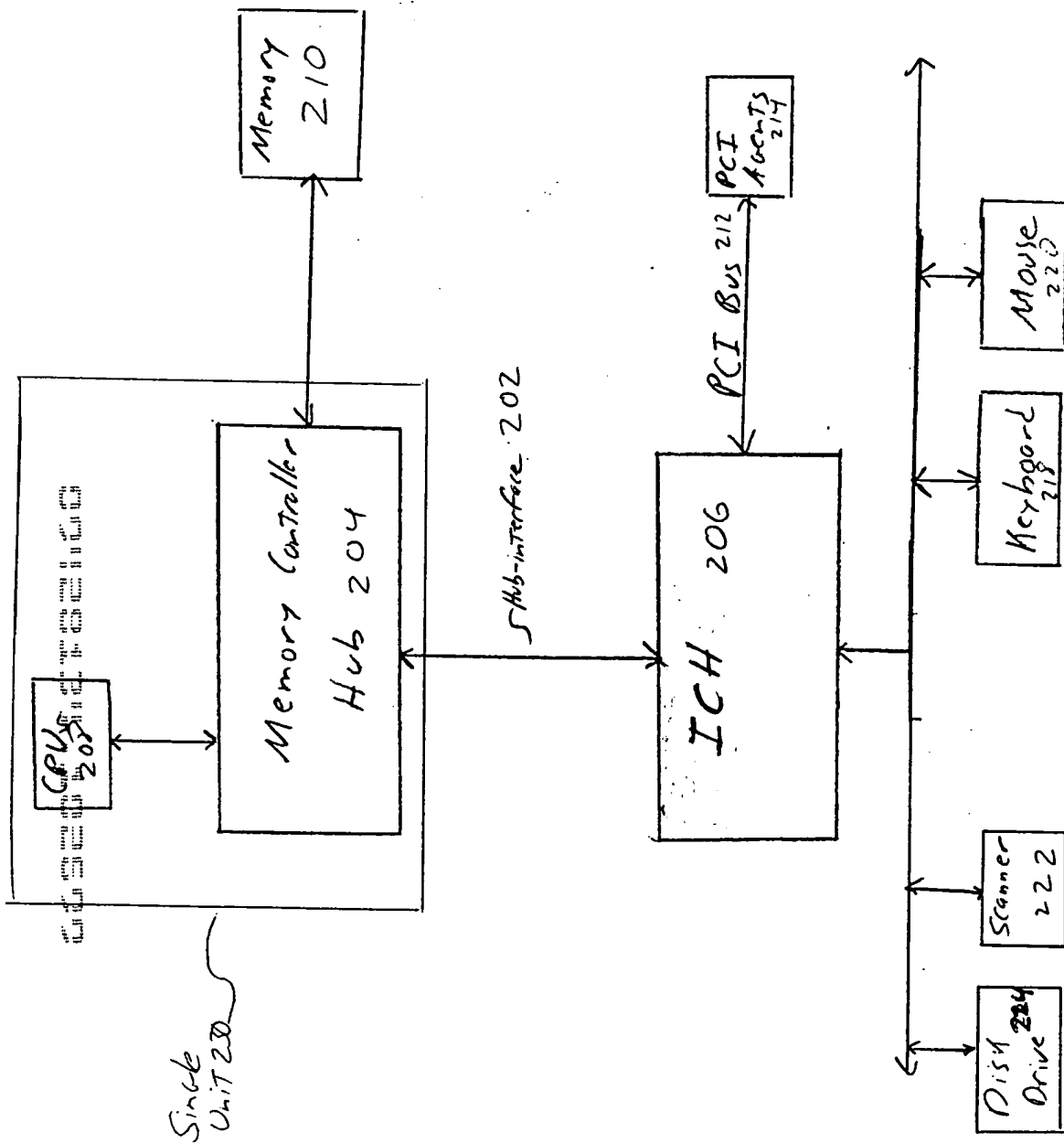


Fig. 11

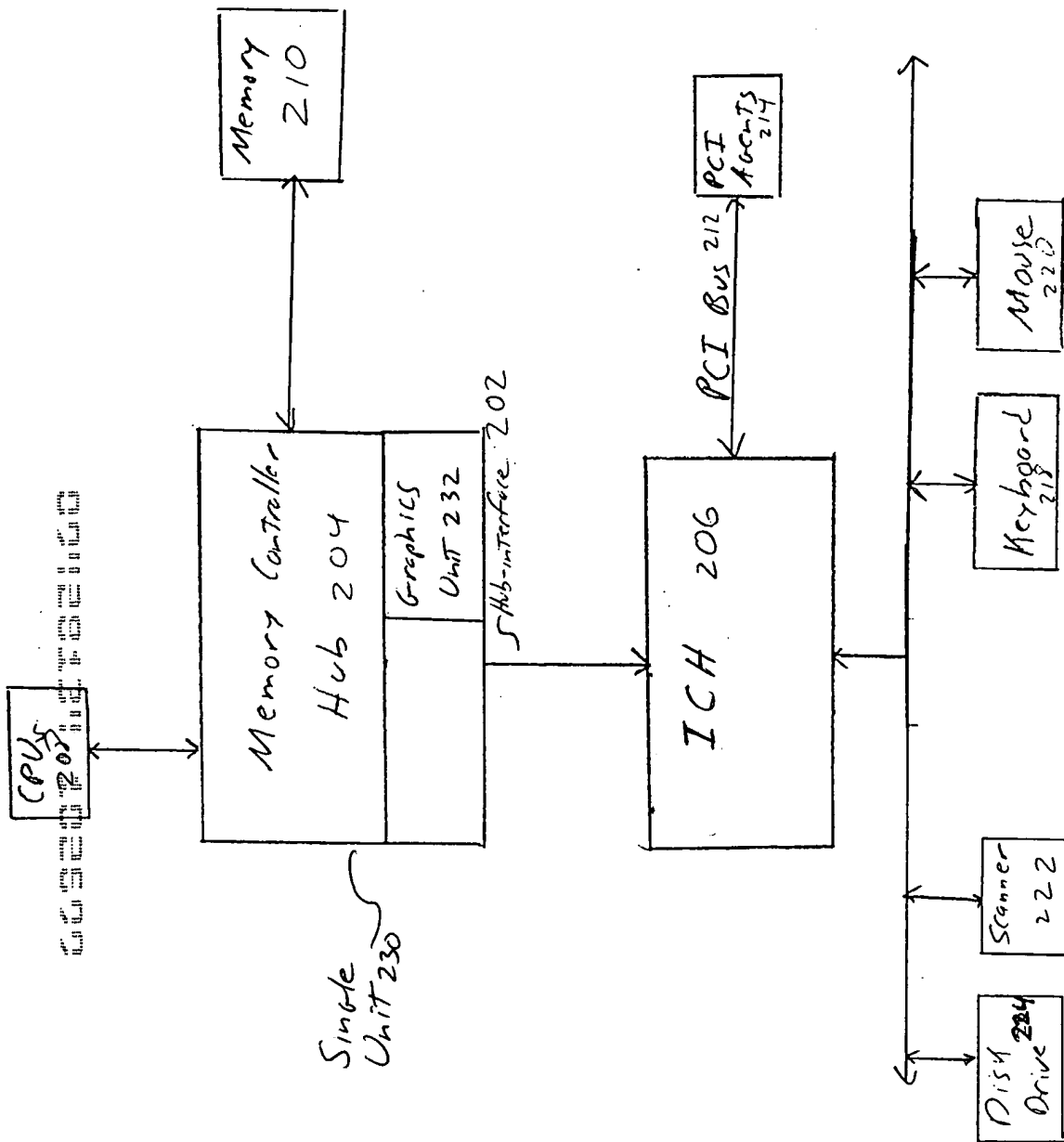


FIG-12